

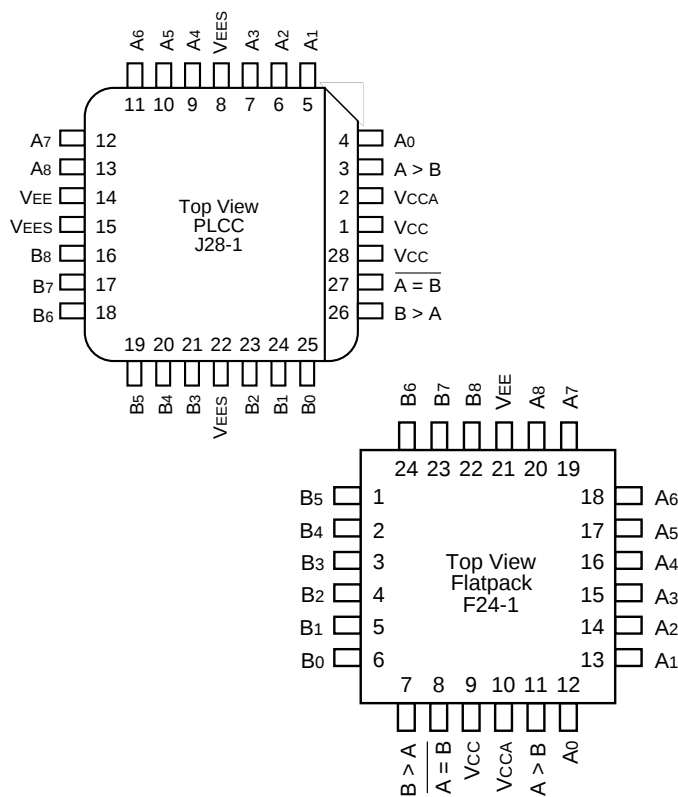
FEATURES

- Max. propagation delay of 1500ps
- IEE min. of -120mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 120% faster than Fairchild
- Approximately 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

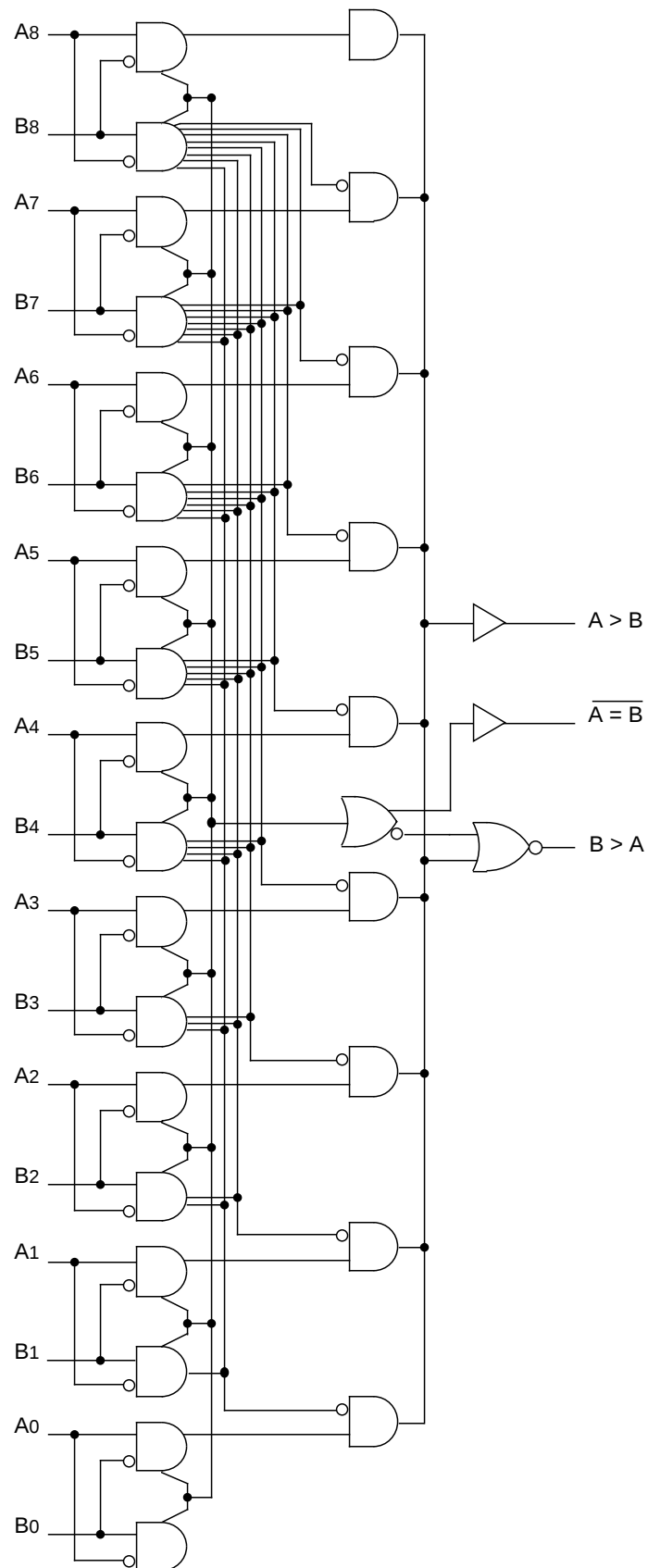
The SY100S366 is an ultra-fast 9-bit magnitude comparator designed for use in high-performance ECL systems. The device compares the arithmetic value of two 9-bit words and indicates whether one word is greater than or equal to the other. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
A0 – A8	A Data Inputs
B0 – B8	B Data Inputs
A > B	A Greater Than B Output
B > A	B Greater Than A Output
$\bar{A} = \bar{B}$	Complement A Equal to B Output (Active LOW)
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

BLOCK DIAGRAM

TRUTH TABLE⁽¹⁾

Inputs									Outputs		
A ₈ B ₈	A ₇ B ₇	A ₆ B ₆	A ₅ B ₅	A ₄ B ₄	A ₃ B ₃	A ₂ B ₂	A ₁ B ₁	A ₀ B ₀	A > B	B > A	A = B
H L L H A ₈ = B ₈ A ₈ = B ₈	H L L H								H L H L	L H L H	H H H H
A ₈ = B ₈ A ₈ = B ₈ A ₈ = B ₈ A ₈ = B ₈	A ₇ = B ₇ A ₇ = B ₇ A ₇ = B ₇ A ₇ = B ₇	H L L H A ₆ = B ₆ A ₆ = B ₆	H L L H						H L H L	L H L H	H H H H
A ₈ = B ₈ A ₈ = B ₈ A ₈ = B ₈ A ₈ = B ₈	A ₇ = B ₇ A ₇ = B ₇ A ₇ = B ₇ A ₇ = B ₇	A ₆ = B ₆ A ₆ = B ₆ A ₆ = B ₆ A ₆ = B ₆	A ₅ = B ₅ A ₅ = B ₅ A ₅ = B ₅ A ₅ = B ₅	H L L H A ₄ = B ₄ A ₄ = B ₄					H L H L	L H L H	H H H H
A ₈ = B ₈ A ₈ = B ₈ A ₈ = B ₈ A ₈ = B ₈	A ₇ = B ₇ A ₇ = B ₇ A ₇ = B ₇ A ₇ = B ₇	A ₆ = B ₆ A ₆ = B ₆ A ₆ = B ₆ A ₆ = B ₆	A ₅ = B ₅ A ₅ = B ₅ A ₅ = B ₅ A ₅ = B ₅	A ₄ = B ₄ A ₄ = B ₄ A ₄ = B ₄ A ₄ = B ₄	A ₃ = B ₃ A ₃ = B ₃ A ₃ = B ₃ A ₃ = B ₃	H L L H A ₂ = B ₂ A ₂ = B ₂			H L H L	L H L H	H H H H
A ₈ = B ₈ A ₈ = B ₈ A ₈ = B ₈ A ₈ = B ₈	A ₇ = B ₇ A ₇ = B ₇ A ₇ = B ₇ A ₇ = B ₇	A ₆ = B ₆ A ₆ = B ₆ A ₆ = B ₆ A ₆ = B ₆	A ₅ = B ₅ A ₅ = B ₅ A ₅ = B ₅ A ₅ = B ₅	A ₄ = B ₄ A ₄ = B ₄ A ₄ = B ₄ A ₄ = B ₄	A ₃ = B ₃ A ₃ = B ₃ A ₃ = B ₃ A ₃ = B ₃	A ₂ = B ₂ A ₂ = B ₂ A ₂ = B ₂ A ₂ = B ₂	A ₁ = B ₁ A ₁ = B ₁ A ₁ = B ₁ A ₁ = B ₁	H L L H A ₀ = B ₀	H L H L	L H L H	H H H H

NOTE:

1. H = HIGH Voltage Level, L = LOW Voltage Level, Blank = X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = -4.2V to -5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current, All Inputs	—	—	200	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-120	-86	-60	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS**CERPACK**

V_{EE} = -4.2V to -5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output	400	1600	400	1600	400	1600	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

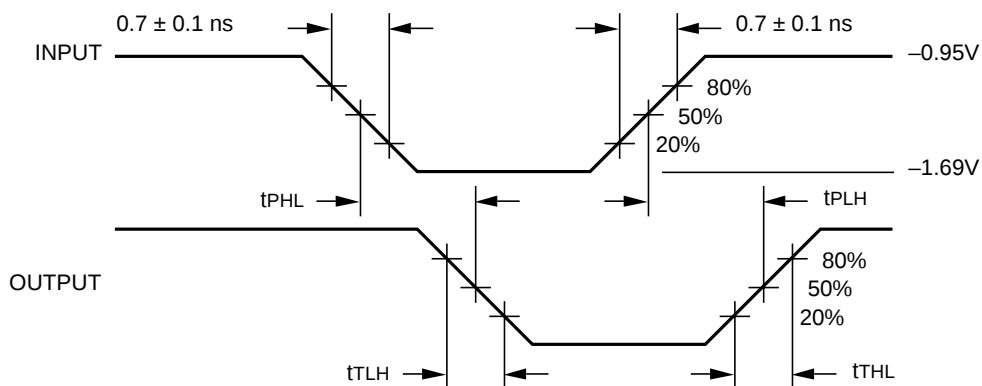
AC ELECTRICAL CHARACTERISTICS

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	400	1500	400	1500	400	1500	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

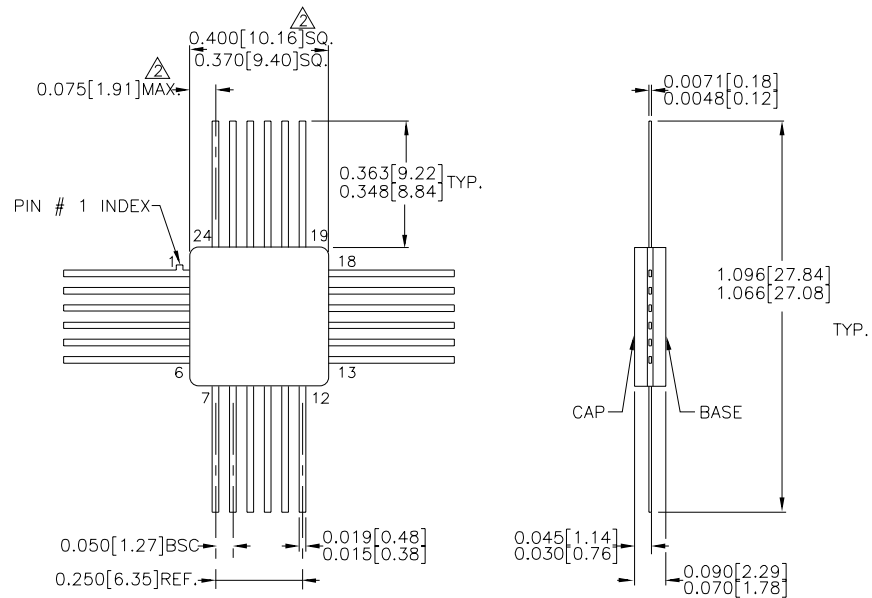
NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S366FC	F24-1	Commercial
SY100S366JC	J28-1	Commercial
SY100S366JCTR	J28-1	Commercial

24 LEAD CERPACK (F24-1)

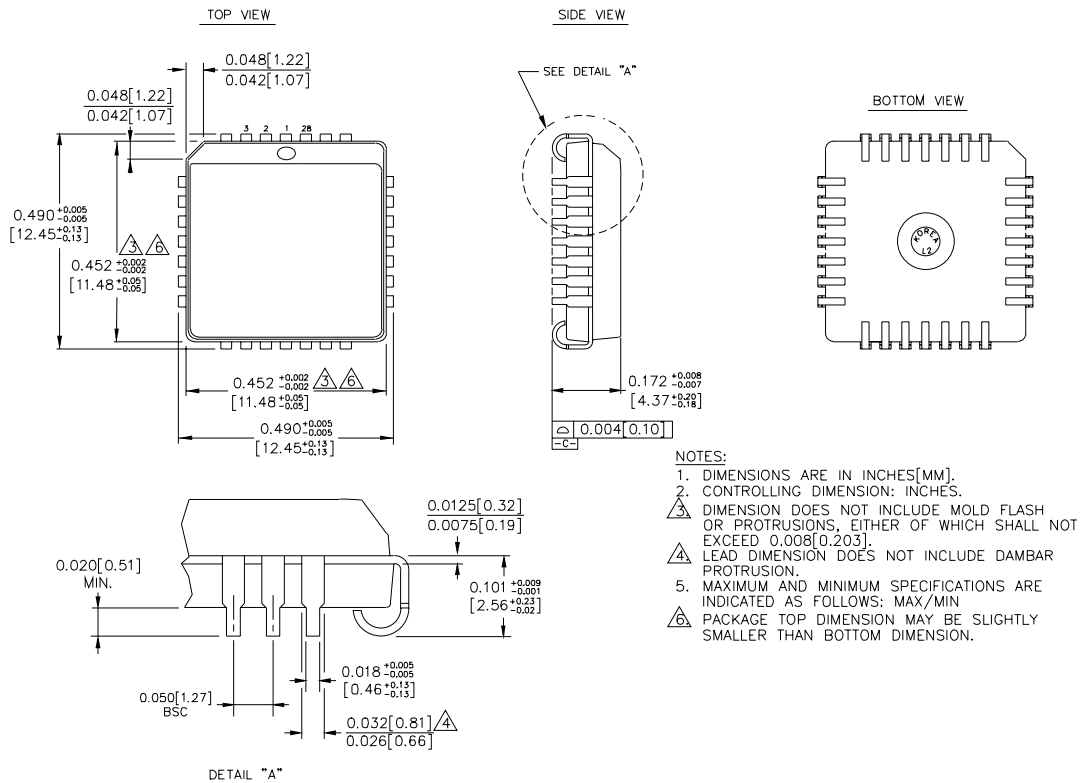


NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28 LEAD PLCC (J28-1)



Rev. 03

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